PERFORMANCE OF MICROWAVE FM SIGNAL FREQUENCY DIVISION CIRCUITS

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Abstract

A comparison between different frequency divider circuits is presented. Both the large-signal behaviour and the transfer properties have been investigated in detail. The results of the computer simulations are supported by experiments.

Introduction

Microwave frequency dividers can find useful applications in quite a lot of areas such as communication systems, PLLs, or for low frequency signal processing. Various concepts for their realization have been proposed in the past: the parametric divider (e.g. /1/), the phase-locked-loop (PLL-) divider /2/, the Miller divider /3/, and the harmonically synchronized oscillator (e.g. /4/).

In this contribution these components have been extensively investigated both theoretically and experimentally. Based on the results obtained, a comparison is made with respect to conversion loss, bandwidth, stability and transfer properties for modulation signals. Because standard techniques have been applied to the analysis, we emphasize here the discussion of the results, along with a short description of the circuits used.

Analysis

A large-signal analysis of the dividers is performed by applying the method of harmonic balance. To this end the device is subdivided into two parts, one representing the nonlinearities involved at the various frequencies considered and the other one the passive embedding circuit. The divider analysis then follows known patterns, which will only briefly be sketched here. The nonlinear sub-network is characterized by a matrix whose elements are generalized describing functions relating the currents and voltages at the different ports. The linear sub-network is described by its admittance matrix. Equating the currents flowing into the nonlinear and into the linear port of the network - this is the condition of oscillation - yields a system of nonlinear equations, the solution of which is the large-signal operating point.

The small-signal analysis is based on the assumption that the operating point is perturbed by low-level signals, which is true for both noise and small modulation signals.Then a parametric approach can be used, where the periodically driven slopes of the nonlinearities are expanded into Fourier series , thus leading to a conversion matrix which describes the mixing process among the various sidebands at the nonlinearity. Relating the small-signal components to the linear circuitry and to their sources by applying Kirchhoffs laws, one obtains a system of linear equations which can easily be solved for the AM and PM sideband powers. The zeros of the corresponding determinant allow to check the stability of the operating point. The small-signal quantities of main interest are the output AM and PM power in the sidebands when AM or PM signals are injected. They are described by the corresponding conversion coefficients.

Parametric Frequency Divider

The circuit model used is described in /1/; Fig. 1 shows the corresponding equivalent circuit. For

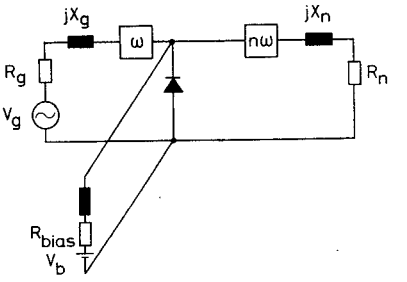

Fig.1: Equivalent circuit of a parametric frequency divider (n = 1/2).

the varactor a quadratic charge-voltage characteristic has been assumed . This component has only been investigated theoretically here. It is, however, well established from various publications about frequency-multipliers (e.g. /5/) that such a simple model gives reliable informations concerning the behaviour of practical circuits.

For the results plotted in Fig. 2, the varactor series resistance was assumed to be 1Ω and the diode Q-factor to be 100; the Q-factors of the bandpass filters in the input and output circuits were set to 10. One big advantage of this dividing circuit is its simplicity. The bandwidth is in the order of 5 % while the conversion efficiency is about 80 % for the special diode Q (Fig. 2 a). To start subharmonic oscillations, a threshold input power must be surpassed. It was found to be half the nominal input power in this case.

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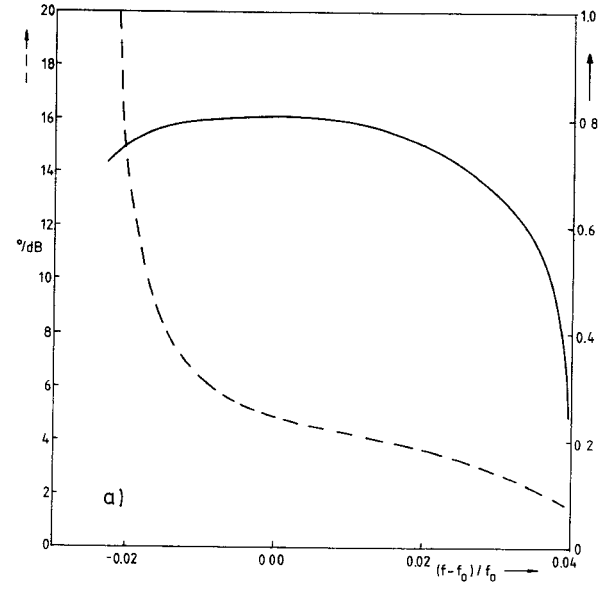
The AM-PM (Fig. 2 a), AM-AM and PM-AM conversions (both in Fig.2 b) have been plotted versus frequency detuning. PM-PM is not shown here because it was found to be -6 dB over the whole tuning range.



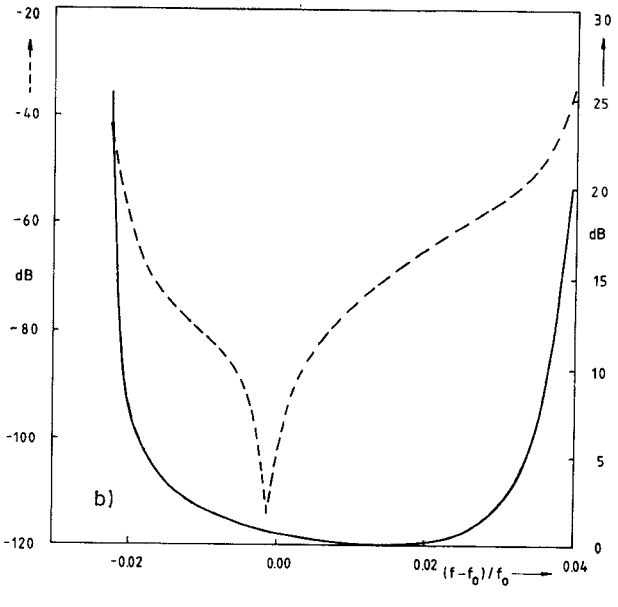


Fig.2: a) Efficiency (——), AM-PM conversion (---) and b) AM-AM (——) and PM-AM (---) conversion of the parametric frequency divider versus frequency detuning.

Subharmonic oscillations abruptly cease at the lower frequency band, where the conversion coefficients show a pole: the divider becomes unstable. No other instabilities could be observered over the tuning range. The AM-PM conversion is almost constant over nearly the total frequency band and stays below 10°/dB. The PM-AM conversion is negligibly small and shows a deep minimum at center frequency. The AM-AM conversion stays slightly above unity, demonstrating the poor limiting capability of the parametric divider.

PLL-Divider

In the PLL-divider circuit, a voltage-controlled oscillator (VCO) provides the output power at the frequency of interest. A sample of the output is fed back, multiplied by the dividing factor n (= 2) and compared with the phase of the input signal in the phase-sensitive detector (PSD). The varactor bias of the VCO is modulated by the amplified PSD output signal thus adjusting the output frequency of the divider. In case of a modulated input signal, the PSD output consists also of a baseband signal modulating the varactor bias. The block diagram of the PLL divider circuit is shown in Fig. 3.

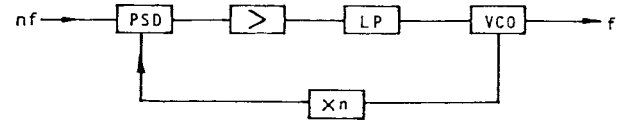


Fig.3: Block diagram of a PLL divide by n circuit; f is the output frequency.

Fig. 4 depicts the measured gain and phase characteristic of the video amplifier (insert). It was

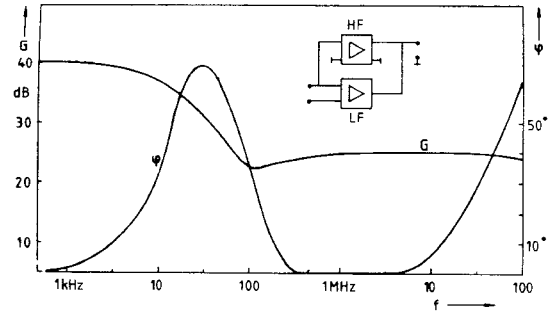


Fig.4: Schematic, gain (G) and phase (φ) characteristic of the video amplifier in the PLL-divider.

designed for low phase shift in the frequency range of interest in order not to increase the total phase shift. The high DC amplification ensures a large hold-in range. In the model the gain characteristic has been approximated by a step function, while the phase shift has been included in the total phase shift - a system parameter which is modeled by a delay time.

The measured bandwidth was slightly less than the calculated one. At an output frequency of f_o = 4.7 GHz, the hold-in range was 270 MHz, the lock-in range 30 MHz. The static loop gain /2/ was approximately $f_g(0)$ = 240 MHz, the dynamic one in a frequency range f_m = 0.1 MHz — 10 MHz still larger than $f_g(f_m)$ = 40 MHz.

The obtainable gain largely depends on the output

power of the VCO. In our experiments we were limited to lower values due to the VCOs available. This is, however, not so important because the high gain capability of PLLs is well established.

The PM-PM transmission factor, which is not shown here, is -6 dB over the tuning range for modulation frequencies $f_m < 10^{-3} \cdot f_o$. This has been confirmed by experiments. The remaining (measured) conversion quantities have been depicted in Fig. 5. The AM-PM stays well below 10 °/dB, while the PM-AM has no influence on the output spectra. The AM-AM finally shows that the PLL is a good limiter.

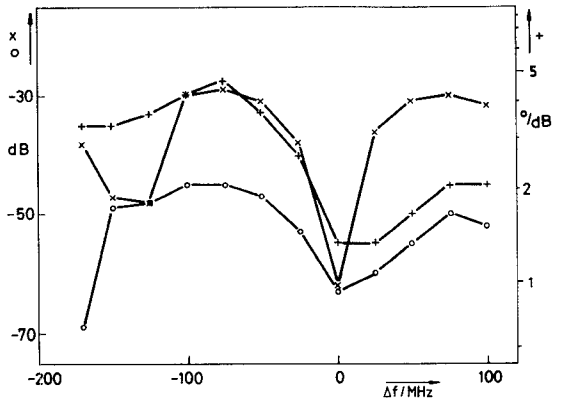


Fig.5: Measured AM-PM (+), AM-AM (x) and PM-AM (o) characteristics of the PLL-divider versus frequency detuning.

These practical results are in principle confirmed by the theoretical analysis, although the latter - due to idealized assumptions for the circuit parameters - promises still better performances. This may be an indication for the main disadvantage of PLL-dividers: the high circuit complexity makes it very difficult to obtain the theoretical limits.

Miller-Divider

The circuit topology of a frequency halver has been sketched in Fig. 6. The output frequency is determined by the mixing product of the input signal and a sample of the output signal at the mixer (M) output port. Behind the bandpass filter (BP) an amplifier must be inserted in order to fulfill the

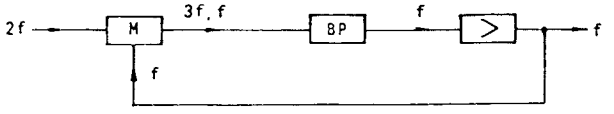


Fig.6: Block diagramm of a Miller-divider; f is the output frequency.

condition for oscillations. The circuit is self-excited if an input signal is applied, which must be above a certain threshold level. This is illustrated in Fig. 7 where the measured output power and gain of an experimental circuit, which has been realized with discrete components, have been plotted versus input power. The bandwidth at maximum gain was only 1 % (f_o = 3.81 GHz), but could be

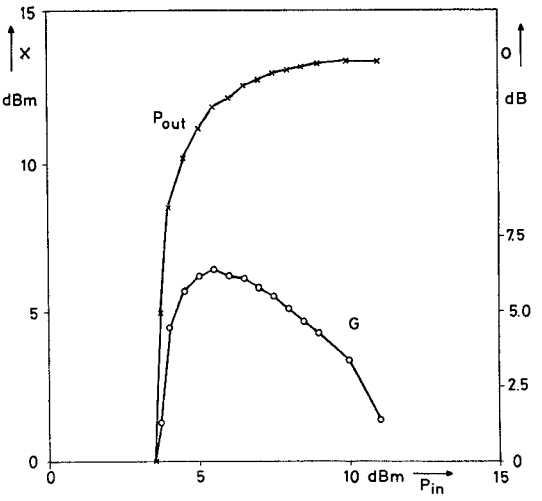


Fig.7: Measured gain and saturation characteristic of the Miller-divider.

increased at the expense of gain. The narrow bandwidth is caused in the experimental circuit, because it has not been optimized. Circuit realizations with a very compact design (e.g. /6/) show that a higher bandwidth is achievable.

Finally, Fig. 8 illustrates the flat output power characteristic of the device and its transfer characteristics over the stable tuning range. The PM-AM conversion is well below -40 dB over nearly the whole tuning range. The computed and measured PM-PM is at -6 dB. It is not shown here. The AM-AM transmission is above -10 dB, an indication of the poor limiting behaviour of the device.

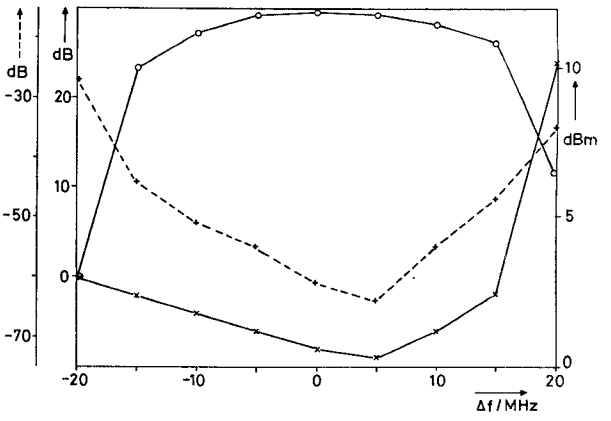


Fig.8: Measured output power (o), AM-AM (x) and PM-AM (+) conversion of the Miller-divider versus frequency detuning.

Due to this relatively high AM-AM conversion, the AM-PM could not be measured with sufficient accuracy. However, our theoretical investigations predict values well below 10 °/dB over nearly the whole tuning range.

Harmonically Synchronized Oscillator

This type of divider circuit is an oscillator which is synchronized at a harmonic frequency, while the power is extracted at the fundamental frequency. A theoretical and experimental investigation of such a divider, using a FET as active element, has recently been reported in detail /7/. For this reason, only some of its essential properties shall briefly be reminded here.

The large-signal behaviour can be characterized by high possible gain and poor bandwidth, both being interchangeable within certain limits. Due to the low-pass behaviour of the parasitics of the FET an increase in frequency deteriorates this figure of merit.

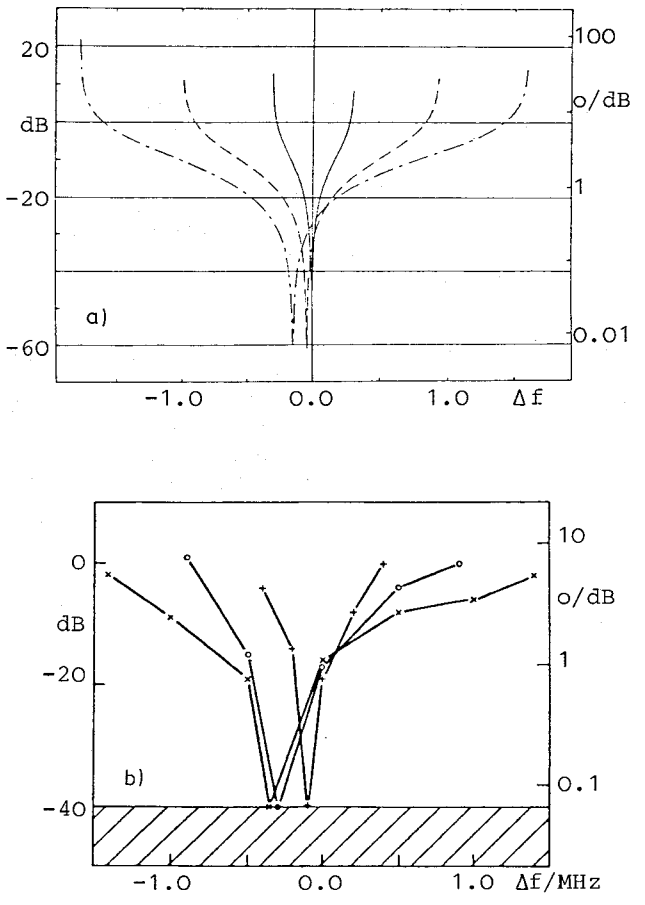


Fig.9: a) Computed and b) measured AM-PM conversion of a harmonically synchronized FET oscillator versus locking range for different gains:
a) G = 15 dB (–.–), 20 dB (---), 30 dB (——);
b) G = 10 dB (x), 15 dB (o), 20 dB (+).

This type of divider also exhibits excellent FM linearity: the PM-PM transmission is -6 dB, the PM-AM conversion being neglectable. Furthermore it shows good AM compression which increases with decreasing injection level and increasing frequency. The AM-PM conversion, which has been plotted in Fig. 9 a, shows a deep minimum at center frequency and stays below 10 °/dB within 90 % of the stable locking range. This is confirmed by experimental results (Fig. 9 b) which have been obtained at K-band frequencies with a fin-line FET oscillator.

Conclusion

To conclude, the main features of the devices presented here are collected in the following table. Poor properties are indicated by "-" or even "--", while "+" and "++" mark good and excellent performances respectively.

	Gain	Bandwidth
Varactor	-	0
PLL	+ +	+
Miller	+	+
Harm. Sync.	+ +	- -

	AM-PM	AM-AM
Varactor	0	- -
PLL	0	+
Miller	0	-
Harm. Sync.	0	+

Acknowledgement

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